TS32MSS64V8D2

144PIN PC100 Unbuffered SO-DIMM
256MB With 16Mx8 CL2

Description

The TS32MSS64V8D2 is a 32M bit x 64 Synchronous Dynamic RAM high-density memory modules. The TS32MSS64V8D2 consists of 16 pieces of CMOS 4Mx8bitsx4banks Synchronous DRAMs in TSOP-II 400mil packages, a 2048 bits serial EEPROM and a PLL on a 144-pin printed circuit board. The TS32MSS64V8D2 is a Dual In-Line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- Burst Mode Operation.
- Auto and Self Refresh.
- Serial Presence Detect (SPD) with serial EEPROM
- LVTTL compatible inputs and outputs.
- Single 3.3V ± 0.3V power supply.
- MRS cycle with address key programs.
  Latency (Access from column address)
  Burst Length (1,2,4,8 & Full Page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.

Pin Identification

Symbol	Function
A0~A11	Address inputs
BA0, BA1	Banks Select
D0~D63	Data inputs/outputs
CLK0	Clock Input
CKE0, CKE1	Clock Enable Input
/CS0, /CS1	Chip Select Input
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write Enable
DQM0~DQM7	DQM
Vcc	Power Supply
Vss	Ground
SDA	Serial Address / Data I/O
SCL	Serial Clock
NC	No Connection

Dimensions

Side	Millimeters	Inches
A	67.60 ± 0.20	2.661 ± 0.008
B	32.80	1.291
C	23.20	0.913
D	4.60	0.181
E	3.30	0.130
F	4.00	0.157
G	20.00	0.787
H	50.50 ± 0.20	1.988 ± 0.008
I	1.00 ± 0.10	0.040 ± 0.004

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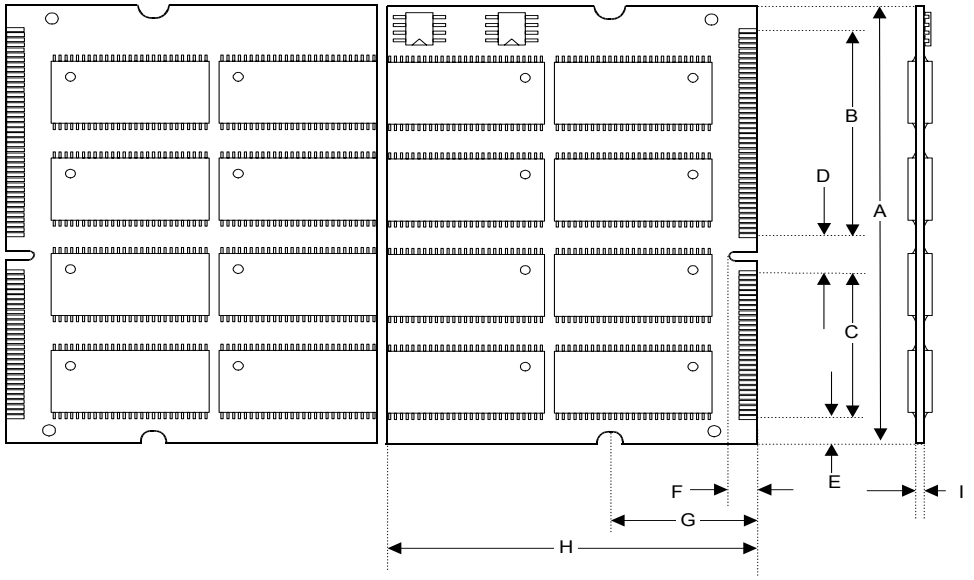


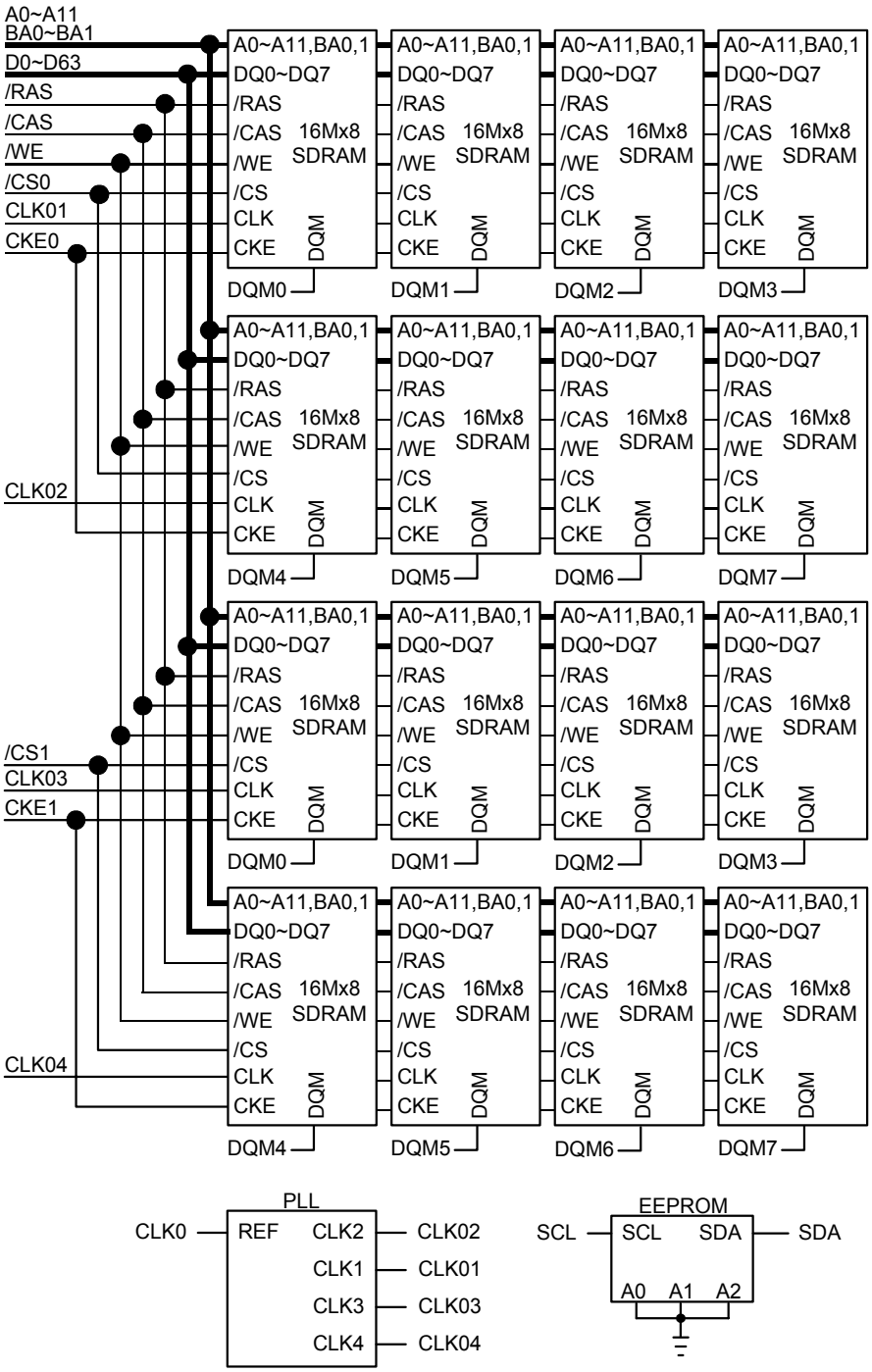
PCB: 09-7265

Pinouts

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	Vss	49	DQ13	97	DQ22	02	Vss	50	DQ45	98	DQ54
03	DQ0	51	DQ14	99	DQ23	04	DQ32	52	DQ46	100	DQ55
05	DQ1	53	DQ15	101	Vcc	06	DQ33	54	DQ47	102	Vcc
07	DQ2	55	Vss	103	A6	08	DQ34	56	Vss	104	A7
09	DQ3	57	*CB0	105	A8	10	DQ35	58	*CB4	106	BA0
11	Vcc	59	*CB1	107	Vss	12	Vcc	60	*CB5	108	Vss
13	DQ4	61	CLK0	109	A9	14	DQ36	62	CKE0	110	*BA1
15	DQ5	63	Vcc	111	A10	16	DQ37	64	Vcc	112	*A11
17	DQ6	65	/RAS	113	Vcc	18	DQ38	66	/CAS	114	Vcc
19	DQ7	67	/WE	115	DQM2	20	DQ39	68	*CKE1	116	DQM6
21	Vss	69	/CS0	117	DQM3	22	Vss	70	*A12	118	DQM7
23	DQM0	71	*/CS1	119	Vss	24	DQM4	72	*A13	120	Vss
25	DQM1	73	NC	121	DQ24	26	DQM5	74	*CLK1	122	DQ56
27	Vcc	75	Vss	123	DQ25	28	Vcc	76	Vss	124	DQ57
29	A0	77	*CB2	125	DQ26	30	A3	78	*CB6	126	DQ58
31	A1	79	*CB3	127	DQ27	32	A4	80	*CB7	128	DQ59
33	A2	81	Vcc	129	Vcc	34	A5	82	Vcc	130	Vcc
35	Vss	83	DQ16	131	DQ28	36	Vss	84	DQ48	132	DQ60
37	DQ8	85	DQ17	133	DQ29	38	DQ40	86	DQ49	134	DQ61
39	DQ9	87	DQ18	135	DQ30	40	DQ41	88	DQ50	136	DQ62
41	DQ10	89	DQ19	137	DQ31	42	DQ42	90	DQ51	138	DQ63
43	DQ11	91	Vss	139	Vss	44	DQ43	92	Vss	140	Vss
45	Vcc	93	DQ20	141	SDA	46	Vcc	94	DQ52	142	SCL
47	DQ12	95	DQ21	143	Vcc	48	DQ44	96	DQ53	144	Vcc

* Please refer Block Diagram

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-1.0~4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0~4.6	V
Storage temperature	TSTG	-55~+150	°C
Power dissipation	PD	16	W
Short circuit current	Ios	50	mA
Mean time between failure	MTBF	50	year
Temperature Humidity Burning	THB	85°C/85%, Static Stress	°C-%
Temperature Cycling Test	TC	0°C ~ 125°C Cycling	°C

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
2. Functional operation should be restricted to recommended operating condition.
3. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	VIH	2.0	3.0	VDD+0.3	V	1,2
Input low voltage	VIL	-0.3	0	0.8	V	1,2
Output high voltage	VOH	2.4	-	-	V	IOH = -2mA
Output low voltage	VOL	-	-	0.4	V	IOL = 2mA

Note : 1.All voltages are referenced to Vss.
2.VIH may overshoot to VDD+2.0V for pulse width of <4ns with 3.3V. VIL may undershoot to -2.0V for pulse width<4.0ns with 3.3V. Pulse width measured at 50% points with amplitude-measured peak to DC reference.

CAPACITANCE (VDD = 3.3V, TA = 23℃, f = 1MHz, VREF = 1.4V ± 200mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A11, BA0~BA1)	CIN1	45	85	pF
Input capacitance (/RAS, /CAS, /WE)	CIN2	45	85	pF
Input capacitance (CKE0~CKE1)	CIN3	25	45	pF
Input capacitance (CLK0)	CIN4	25	21	pF
Input capacitance (/CS0~/CS1)	CIN5	25	25	pF
Input capacitance (DQM0~DQM7)	CIN6	10	15	pF
Data input/output capacitance (DQ0~DQ63)	COUT	13	18	pF

DC CHARACTERISTICS

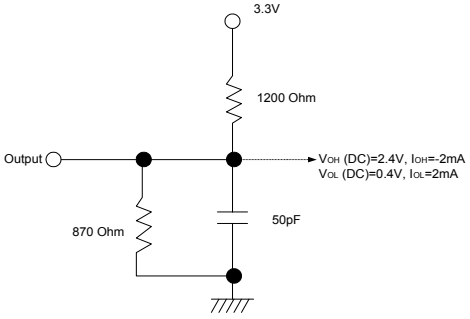
(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Value	Unit	Note
Operating Current (One Bank Active)	ICC1	Burst Length =1 tRC≥tRC(min) IOL=0mA	960	mA	1
Precharge Standby Current in power-down mode	ICC2**P**	CKE≤VIL(max), tCC=10ns	32	mA	
	ICC2**PS**	CKE & CLK≤VIL(max), tCC=∞	32		
Precharge Standby Current in non power-down mode	ICC2**N**	CKE≥VIH(min), /CS≥VIH(min), tCC=10ns Input signals are changed one time during 20ns	320	mA	
	ICC2**NS**	CKE≥VIH(min), CLK≤VIL(max), tCC=∞ Input signals are stable	160		
Active Standby Current in power-down mode	ICC3**P**	CKE≤VIL(max), tCC=10ns	80	mA	
	ICC3**PS**	CKE & CLK≤VIL(max), tCC=∞	80		
Active Standby Current in non power-down mode (One Bank Active)	ICC3**N**	CKE≥VIH(min), /CS≥VIH(min), tCC=10ns Input signals are changed one time during 20ns	480	mA	
	ICC3**NS**	CKE≥VIH(min), CLK≤VIL(max), tCC=∞ Input signals are stable	400		
Operating Current (Burst Mode)	ICC4	IOL= 0 mA Page Burst tccD = 2CLKs	1040	mA	1
Refresh current	ICC5	tRC≥tRC(min)	1760	mA	2
Self Refresh Current	ICC6	CKE≤0.2V	32	mA	

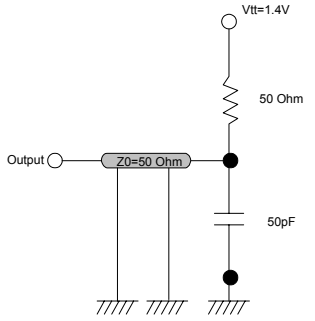
Note: 1. Measured with outputs open.
2.Refresh period is 64ms.
3.Unless otherwise noticed, input swing level is CMOS (VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (VDD=3.3±0.3V, TA=0 to 70°C)

Parameter	Value	Unit
AC Input levels (VIH/VIL)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf=1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Value	Unit	Note
Row active to row active delay	tRRD(min)	20	ns	1
/RAS to /CAS delay	tRCD(min)	20	ns	1
Row precharge time	tRP(min)	20	ns	1
Row active time	tRAS(min)	50	ns	1
	tRAS(max)	100	us	
Row cycle time	tRC(min)	70	ns	1
Last data in to new col. address delay	tCDL(min)	1	CLK	2
Last data in to Active delay	tDAL(min)	2CLK+ tRP	-	
Last data in to row precharge	tRDL(min)	2	CLK	2
Last data in to burst stop	tBDL(min)	1	CLK	2
Col. address to col. address delay	tCCD(min)	1	CLK	3
Number of valid output data		1	ea	4

Note: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter	Symbol	Value		Unit	Note
		Min	Max		
CLK cycle time	tCC	10	1000	ns	1
CLK to valid output delay	tSAC		6	ns	1, 2
Output data hold time	tOH	3		ns	2
CLK high pulse width	tCH	3		ns	3
CLK low pulse width	tCL	3		ns	3
Input setup time	tSS	2		ns	3
Input hold time	tSH	1		ns	3
CLK to output in Low-Z	tSLZ	1		ns	2
CLK to output in Hi-Z	tSHZ		6	ns	

Note: 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5) ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)= 1ns.
if tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_0~A_9	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down	Entry		H	L	H	X	X	X	X	X			
					L	V	V	V					
	Exit		L	H	X	X	X	X	X				
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X	X			
					L	H	H	H					
	Exit		L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note:
1. OP Code: Operand Code
   A_0~A_{11}, BA_0~BA_1: Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatically precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA_0~BA_1: Bank select address.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
   If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command cannot be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edged of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Serial Presence Detect Specification

Serial Presence Detect								
Byte No.	Function Described	Standard Specification	Vendor Part					
0	Number of Bytes Written into Serial Memory	128bytes	80					
1	Total Number of Bytes of S.P.D Memory	256bytes	08					
2	Fundamental Memory Type	SDRAM	04					
3	Number of Row Addresses on this Assembly	12	0C					
4	Number of Column Addresses on this Assembly	10	0A					
5	Number of Module Banks on this Assembly	2 banks	02					
6	Data Width of this Assembly	64bits	40					
7	Data Width Continuation	0	00					
8	Voltage Interface Standard of this Assembly	LVTTL3.3V	01					
9	SDRAM Cycle Time (highest CAS latency)	10ns	A0					
10	SDRAM Access from Clock (highest CL)	6ns	60					
11	DIMM configuration type (non-parity, ECC)	DIMM	00					
12	Refresh Rate Type	15.625us/Self Refresh	80					
13	Primary SDRAM Width	X8	08					
14	Error Checking SDRAM Width	0	00					
15	Min Clock Delay Back to Back Random Address	1 clock	01					
16	Burst Lengths Supported	1,2,4,8 & Full page	8F					
17	Number of banks on each SDRAM device	4 bank	04					
18	CAS # Latency	2, 3	06					
19	CS # Latency	0 clock	01					
20	Write Latency	0 clock	01					
21	SDRAM Module Attributes	Non Buffer	00					
22	SDRAM Device Attributes: General	Prec All, Auto Prec, R/W Burst	0E					
23	SDRAM Cycle Time (2nd highest CL)	10ns	A0					
24	SDRAM Access from Clock (2nd highest CL)	6ns	60					
25	SDRAM Cycle Time (3rd highest CL)	-	00					
26	SDRAM Access from Clock (3rd highest CL)	-	00					
27	Minimum Row Precharge Time	20ns	14					
28	Minimum Row Active to Row Activate	20ns	14					
29	Minimum RAS to CAS Delay	20ns	14					
30	Minimum RAS Pulse Width	50ns	32					
31	Density of Each Bank on Module	128MB	20					
32	Command/Address Setup Time	20ns	20					
33	Command/Address Hold Time	10ns	10					
34	Data Signal Setup Time	20ns	20					
35	Data Signal Hold Time	10ns	10					
36-61	Superset Information	-	00					
62	SPD Data Revision Code	INTEL	12					
63	Checksum for Bytes 0-62	17	17					
64-71	Manufacturers JEDEC ID code per JEP-108E	Transcend	7F, 4F					
72	Manufacturing Location	T	54					
73-90	Manufacturers Part Number	TS32MSS64V8D2	54	53	33	32	4D	53
			53	36	34	56	38	44
			32	20	20	20	20	20

91-92	Revision Code	-	0
93-94	Manufacturing Date	By Manufactory	Variable
95-98	Assembly Serial Number	By Manufactory	Variable
99-125	Manufacturer Specific Data	-	0
126	Intel Specification Frequency	-	64
127	Intel Specification CAS# Latency/Clock Signal Support	CL=2,3 Clock 0	C6
128~	Unused Storage Locations	Open	FF